| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/066,539 | LIEN ET AL. | |
| | Examiner | Art Unit | |
| | JOHN J. TABONE JR | 2117 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment and arguments filed 01/08/2008*.

2. ☒ The allowed claim(s) is/are *6-18*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *02052008-A* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Jacques Louis-Jacques
JACQUES LOUIS-JACQUES
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

## DETAILED ACTION

1. Claims 1-5 ~~are currently pending in the application and~~ have been cancelled. JLJ 2/11/08

Claims 6-18 are newly added and have been examined.

### *Continued Examination Under 37 CFR 1.114*

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/08/2008 has been entered.

### *Response to Arguments*

3. Applicant's arguments filed 01/08/2008 with respect to claims 6-18 have been fully considered and are persuasive. The Final Rejection of 07/10/2007 has been withdrawn.

## EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided

by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney Kenneth D'Alessandro's assistant, Stephanie Davis, on 02/05/2008.

The application has been amended as follows:

Replace the **Abstract** in it entirety with the following:

A method for testing FPGA routing circuitry having a plurality of first sets of tracks having programmably connectable individual track segments includes providing a global control signal to simultaneously turn on all of the programmable elements in at least two of the first sets of tracks, defining individual test inputs to apply to the first end of each of the at least two of the first sets of tracks, determining an expected logic result for a selected logical combination of the individual test inputs, applying the individual test inputs to the first end of each of the at least two of the first sets of tracks, performing the selected logical combination on the second ends of the at least two of the first sets of tracks to generate an actual logic result, and flagging an error if the actual result is not identical with the expected logic result.

**Claim 6**, line 1; Change "the routing circuitry" to "a routing circuitry".

**Claim 6**, line 3; Change "each set of first tracks" to "each first set of tracks".

***Allowable Subject Matter***

5. **Claims 6-18** are allowed.

The following is an Examiner's Statement of Reasons for Allowance:

The present invention relates to testing the routing or interconnect resources of an FPGA.

The claimed invention as set forth in **claim 6** (broadest claim) recites features such as:

A method for testing a routing circuitry in a field programmable gate array (FPGA) having a first FPGA tile, the routing circuitry having a plurality of first sets of tracks running in a first direction, each set of first tracks having a plurality of individual track segments that are programmably connectable to one another between a first end and a second end by individual programmable elements, the method comprising:

providing a global control signal to simultaneously turn on all of the programmable elements in at least two of the first sets of tracks;

defining individual test inputs to apply to the first end of each of the at least two of the first sets of tracks;

determining an expected logic result for a selected logical combination of the individual test inputs to the at least two of the first sets of tracks;

applying the individual test inputs to the first end of each of the at least two of the first sets of tracks;

performing the selected logical combination on the second ends of the at least two of the first sets of tracks to generate an actual logic result; and

flagging an error if the actual result is not identical with the expected logic result.

The prior arts of record teach a method for testing the interconnect in an FPGA, and the claimed steps of defining individual test inputs, determining an expected logic result, applying the individual test inputs, performing the selected logical combination and flagging an error; **Das et al.**, (A low cost approach for detecting, locating, and avoiding interconnect faults in FPGA-based reconfigurable systems) is one example of such prior arts. (See pg. 268, section 3.2, Steps 1-6).

The prior arts of record, however, fail to teach, singly or in combination, *providing a global control signal to simultaneously turn on all of the programmable elements in at least two of the first sets of tracks.* In other words, the simultaneous activation of the switches in the present invention is performed to make a complete circuit from one end of a set of routing tracks to another end of the set of routing tracks for the purpose of testing the continuity of the set of routing tracks. As such, modification of the prior art of record to include the claimed *global control signal* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *global control signal* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *global control signal* as set forth in **claim 6**. Hence, **claims 6-18** are allowable over the prior arts of record.

The Examiner agrees with the Applicant's arguments with regard to this feature in view of the arts of record; therefore, the Examiner favors the allowance of **claims 6-18**. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

**Renovell, et al.**, Testing the configurable interconnect/logic interface of SRAM based FPGA's, IEEE, 9-12 March 1999 Page(s):618 – 622, teaches testing the configurable modules that interface the global interconnect and the logic cells of an SRAM-based FPGA.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN J. TABONE JR whose telephone number is (571)272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JACQUES H. LOUIS JACQUES can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr. 1/8/08
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